IJAREEIE

e-ISSN: 2278-8875
p-ISSN: 2320-3765

# International Journal of Advanced Research

## in Electrical, Electronics and Instrumentation Engineering

Volume 11, Issue 2, February 2022

INTERNATIONAL STANDARD SERIAL NUMBER INDIA

Impact Factor: 7.282

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.282|

|| Volume 11, Issue 2, February 2022 ||

DOI:10.15662/IJAREEIE.2022.1102001

# A Clock Routing Technique Based on Thiessen Polygons and Dirichlet Tessellation

**Amit Kumar**

Cadence Design Systems, 2655 Seeley Avenue, San Jose, CA, USA

**ABSTRACT**: This research presents a work in progress towards the advancement of these two goals. The Hybrid mesh network distribution systems that have been proposed in the past utilize tree and non-tree networks to help deal with density account; therefore, they are likely to lead to unnecessary high-power consumption and skewness in mesh distribution networks. The method proposed in this research is the integration of sink densities in the design, an aspect that has not been explored in the past. Dirichlet tessellation and Thiessen polygons methodologies are used in the design of the upper mesh. In between the Mesh and the sinks is a binary tree formation, which feeds the mesh. The sinks are organized in clusters which are within k polygons, on the lower level of the clock network. Data analysis of this new prototype indicates that it has the potential to reduce skewness and delay.

**KEYWORDS:** Clock routing, computational geometry, clock tree synthesis.

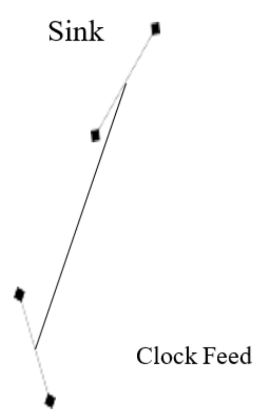
## I. INTRODUCTION

Clock distribution networks are not uniform but rather appear as a randomized function when traced on a lattice. In a definitive diagram, the clock network is represented by sinks which appear as randomized dots on lattices. There have been continuous efforts to improve clock distribution networks, through different layouts for clock signals. This task is made difficult by the large number of transistors that are in a single chip and the rise in the densities of chips. The two most prevalent layouts for clock signals are the local distribution and the global network distributions. The difference between them arises from the sources of their clock signals and their target distribution destination. For the local distribution, their source of the clock signal is the clock sinks and they dispense these signals to the global networks of the clock. On the other hand, the global networks, their source is the clock feed and their target relay point is the local regions. Empirically, there are three categories to which clock networks can be put into and are analyzed below.

Tree-based networks

Figure 1 below shows the structure of a tree-based network. This kind of network is preferred for the simplicity that goes into its design and simulation. The other reason this kind of network is proffered is that it has a low consumption of power.

Figure 1: Tree based network



| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.282|

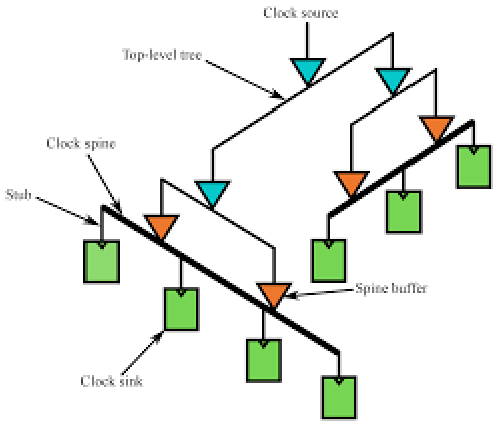
|| Volume 11, Issue 2, February 2022 ||

DOI:10.15662/IJAREEIE.2022.1102001

Non tree based networks

Figure 2 below shows the non tree based network layout. The con tree based networks are more complex as compared to the tree based networks due to their extensive wiring. These elaborate connection leads to increased power consumption.

Figure 2: Non tree based network




Hybrid networks

In the recent past, there have been efforts to create a hybrid network system that adapts the non-tree and tree-based network structure. In this hybrid system, the mesh of the structure is constituted of a non-tree part, while the network is crafted out of a tree structure. Hybrid systems can be classified as either lower-level mesh structures or upper-level mesh structures.

Lower-level mesh structures

Low-level mesh structures are preferred for use in local routing. In their connections, the sinks are usually connected to me mesh without any routing. Their basic structure is such that it has a low-level mesh whose equilibrium is forged at multiple points by a binary tree. To perform global routing, there is the use of an upper-level balanced tree structure.

Upper-Level-Mesh Structure

The upper-level mesh structure is a recent invention in the mesh structure. First, for local routing purposes, there is the use of sinks that are tethered to tree-based structures. An upper-level mesh is used to anchor the roots of the trees. For global routing, an upper-level mesh structure with a diagonal orientation is used. Figure 4 shows an upper-level Mesh structure. The advantage of the upper-level mesh structure over the low-level mesh structure is that it has a lower power consumption.  However, if too many sinks are placed on this structure it can lead to skewness since it does not take the density of sinks into account.

Upper-Level-Mesh Structure

The need for a new structure is inspired by two challenges identified in the Upper-Level-Mesh Structure. The first is that it does not take into account the distribution of sinks. There is a uniform mesh for all distributions of sinks. The downside of this structure is that it leads to the consumption of more power. Structures that have a mesh that is based on the distribution of the sinks tend to consume less power. Some areas may have little or no sinks and they still have large mesh structures and these consume energy that should not be consumed.

The proposed multi-level clock routing scheme

This research presents a new prototype that can be used in place of the ones discussed above. The major focus of the new prototype is to ensure that the mesh has little or no skewness. One of the structural changes in the new prototype is that it has a balanced tree structure that feeds the mesh network and it emanates from the source of the clock. The principle that is applied is the Dirichlet tessellation and its used to modulate Thiessen polygons. This principle has a parameter called k, which represents the number of partitions in the multi-level routing scheme. The value of K is assigned so that it is congruent with the number of sinks; n. The larger the value of K, the larger the amount of power

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.282|

|| Volume 11, Issue 2, February 2022 ||

DOI:10.15662/IJAREEIE.2022.1102001

that will be consumed, and the larger the skewness that will be recorded as well. For each sink that is within a certain polygon, it is located near the center of the polygon. All the sinks within the structure are then connected through a tree-based network.

One of the merits of this design is that it has low skewness. This is because there are few sinks in the clock tree. The sinks in the tree are connected through the use of a routing method and they do form clusters together. Further, each of the clusters is connected to a spine that is the most proximal to the cluster. Another contributor to low skewness is an increase in value of k which leads to a consequent decline in the number of sinks. The reduced size of the clock tree is due to an increase in spines is also a reason why there is low skewness in this model. An increase in the number of spines leads to a reduction in the size of the clock tree. The third reason there is low skewness is because of the perpendicular bisectors that join different clusters. All the clusters are joined by perpendicular bisectors. The perpendicular bisectors are located at the same distances from the sinks that are at the middle of the clusters. As such, for any bisector, it has equal distances from the generation points. This makes the signals that are generated by the clock travel the same distance to get to the generating points on all the bisectors. This symmetry in the signal travel leads to skewness as well. The combination of the three above factors that contribute to low skewness leads to an overall low skewness of the new prototype as compared to the other previous structures.

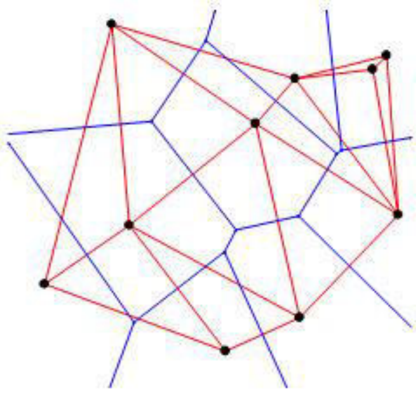
This paper focuses on the dynamics of the development of the prototype whose breakdown has been given. The most critical aspects that are analyzed are the routing schemes that will be used in the prototype, the spine placement process, the metrics behind sprouts and their correlation with skewness, how to deal with errors that are a function of outliers, and the cluster optimization process. There will be optimization for the porotype discussed and the analysis of this optimization will be presented in the paper as well.

## II.OVERVIEW OF CLOCK ROUTING SCHEME

Theoretical background

It is critical to find a way to optimize mesh distribution in a clocking scheme. This is because, as much as the mesh is known to reduce the skewness of clocks, they are also responsible for the consumption of a lot of power. The mesh structure is construed in a polygon structure. The optimization of the polygon structure will be using the *Thiessen polygons* theoretical framework. The focus of this optimization is to keep the polygons at a minimum while ensuring that clock skewness stays at or close to zero. For each of the sinks in a clock network, they for a Delaunay Triangulation with two other sinks in the lattice to form independent triangles. Conventionally, each of the sinks has a pseudo connection to five other sinks in the lattice to make other independent Delaunay Triangulation. This triangulation is used with *Thiessen polygons* to minimize the wire mesh used in the clock network. The *Thiessen polygons* are tetrahedrons in nature and they form a lattice whose structure is a function of the pseudo sink connections as shown in figure 3 below.

Figure 3: Delaunay Triangulation in blue color and Thiessen polygons in red color



Based on the illustration above, each of the sinks is surrounded by a blue Thiessen polygon, and the region that makes up this polygon is called the Thiessen polygons region. Each of the blue lines of the polygon is called the Thiessen polygons edges and they terminate at *Thiessen polygons vertices*. The position of the Thiessen polygons edges is such that they are equidistant from the two sinks for which they are responsible for forming a boundary. This boundary line

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.282|

|| Volume 11, Issue 2, February 2022 ||

DOI:10.15662/IJAREEIE.2022.1102001

is perpendicular to the line that joins the two sink points. As such all the points on the boundary are equidistant from the two sinks which they divide with a perpendicular boundary.

Process 1: Process of making the network distribution
The prototype process of the networking is linear. The first step is to trace out all the sinks in the distribution network. The second step is to decide on the number of polygons that will be constructed for the number of sinks that have been identified. This is done through the use of an algorithm. The third step is to construct the *Thiessen polygons.* To do this, perpendicular bisectors are drawn between sinks. The perpendicular bisectors are drawn in such a way that they are equidistant from two corresponding sink points. These perpendicular lines form the Thiessen polygons edges. Spines are placed on the edges of the Thiessen polygons edges to connect them to form *Thiessen polygons.* The fourth step is to construct the tree structure. First, spines that emanate from the mesh to the sinks are constructed. The spines are made at multiple points with the help of the binary tree structure. The spines emanate from the edges of the spines. The spines move from the mesh and extrude to the sink clusters. To construct a balanced tree structure, all the sinks that are adjacent to each other are connected. A tree-based routing scheme is used to make this connection. Sinks that are located within the proximity of a spine form a cluster. For each cluster, its most central point is its roots and it is from this root that the spine will be connected. These cluster's roots are connected to the spines that are most proximal to them, and attached to the edges.

**Procedure 2: Process of constructing the cluster center for the sink**
This procedure assumes that there are n sinks in the clock, representing the network distribution. For these sinks, there are k partitions constructed. For K partitions, there will be k spines that will be constructed. The first step in finding the centers of the sinks is to generate some random k points where the spines will emanate from and join with the clusters. The second step is that for each all the sinks in the distribution, the distance of each of the sinks from these points is calculated, and these will be the reference points. The third step is to divide the sink points into clusters. This is done by making sure that all the sinks that are close to a certain reference point are allocated to a similar cluster. The fourth step is that the mean distances between the sinks and the reference are then calculated. Fifth is that the calculated mean should be equal to the mean of the reference points. Sixth, if this is not so, then some new reference points should be taken and the process repeated until the mean of the clusters is equal to the mean of the reference points. This process would then be repeated from step 3 until there two measures are similar.
Problem sample Thiessen's polygons concept has the overall objective of determining the number of polygons that will be in a clock network. The number of the polygons used is highly dependent on the criterion that is used to formulate the polygons. The method that is most befitting for the clock distribution network is the Manhattan distance method. The Manhattan distance method holds that the distance between two points is the sum of the absolute difference in vectors of the two points. The reason for the use of this method is that the working bench of a clock network is gridded and can only work with orthogonal dimensions. For a clock that has n sinks, it was assigned K polygons in procedure 2. In procedure 2, the number of random points chosen was k and it has no consequence on the process. The process is usually automated and is done through the use of an algorithm. As such, any choice that is made on the K random points will only change the number of alterations that the algorithm will need to process. As stated in procedure 2, the alterations happen from step 3 to step 6. After running the algorithm, the value that is obtained is the cluster mean and it is used in the construction of a Dirichlet tessellation.

## III.CONCEPT OF SPROUTS

Sprouts are extensions of a spine. This normality happens during the computational of the mean of the cluster. It happens that sometimes, the mean of the cluster that is computed is larger than the distance from the spines to the center of the cluster. Sprouts can be classified as either spine sprouts or they can be classified as edge sprouts. For the spine sprout, there is an extension of the spine such that there is zero skewness for any point on the sprout. Secondly, the spine sprout leads to centers of the clusters being at an ideal location distance. On the other hand, the edge sprout is located at the edge of the wire mesh. Its main drawback is that it leads to the use of excess wire length, which can raise the cost.

*Incomplete Cell* - cells are the convex polygons that are formed by the Thiessen polygons. The term cell is adapted from the fact that the sinks that are within the polygons appear as nuclei of the polygons. Before a polygon is drawn, a cell usually has infinite dimensions on all sides. However, after the cell has been made, it becomes bonded on all sides based on the perpendicular boundaries that it makes with other cells. However, there are times when the boundaries that are made on a cell are not complete due to the orientation of the cell relative to other cells and the boundaries that are drawn on it. Such a cell is called an Incomplete Cell. For this type of cell, there is a need to find a way to make it complete, since there cannot be a disconnect in a mesh structure. Outlier points -In any incomplete Cell the connection of the mess and the sinks are based on the center of the cluster. Sometimes, there may be some points that are very far from the mean distances calculated for the cluster. These distant points are regarded as outlier points. In some instances, there might be more than one outlier point. Outlier points lead to a very high skewness level. As such, outliers should be removed to remove skewness. In dealing with the outlier points, two methods can be used. The first is through the use of sub-connections to the spine. Through the use of

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.282|

|| Volume 11, Issue 2, February 2022 ||

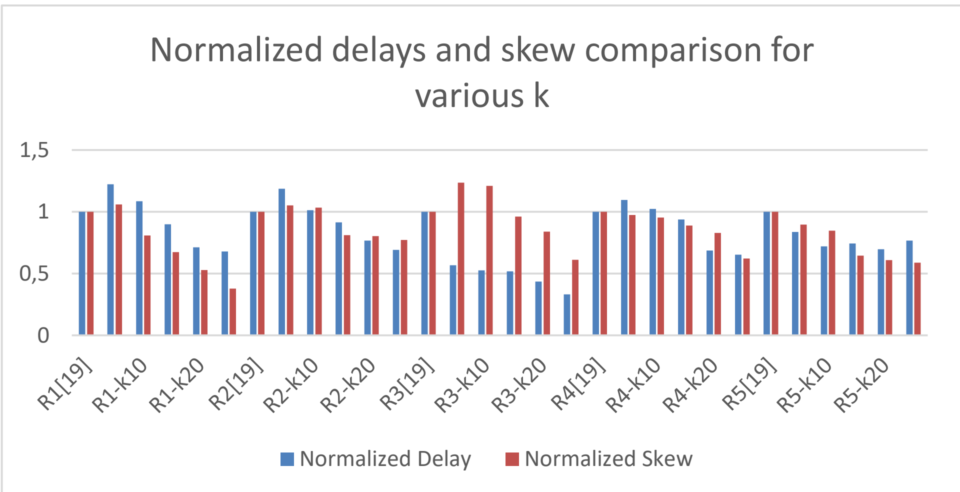
DOI:10.15662/IJAREEIE.2022.1102001

this method, another center is introduced which will cater to the outlier points. The first step in doing this is to first introduce a random point on the cell. This will act as the center for the outlier point or points based on their distribution. The new center that was introduced could end up serving more than the outlier point. The next step is to introduce a perpendicular bisector to the two centers. Finally, the two centers are connected with spines to the edges of the cell that are most proximal to them. Another process for taking care of the outlier points is to find a way to make a connection that is direct to the mesh network. This is done if the outlier points are located close to the mesh network. However, this method is not the most recommended. The reason it's not recommended is that it uses extra wire to implement and this leads to additional costs of using extra wires. Optimization of cluster sizes --The Thiessen polygons method has utilized the Manhattan method of finding the cluster diameter. In the use of this method, there may be some of the clusters whose diameters are too large. This makes the cluster sizes to be uneven, with some of them being too large while others being too small. Optimization of cluster sizes is about ensuring there is evenness in the cluster sizes. There are several ways in which the cluster sizes can be made to be more even. One of them is through identifying the ideal limit of a cluster and using the sub-method to break down any cluster that is beyond this limit. For instance, the diameter of a cluster could be given a limit of d and if a cluster has a diameter that is larger than this, it can be broken down using the 'sub' method analyzed earlier.
In some instances, a cluster may be too small. Very small clusters are likely to lead to an increase in the number of spines that are used in the connection. The solution for small clusters is to merge two or more small clusters that are neighboring, to make one larger cluster. It must be ensured that the two clusters that are merged have a combined diameter that is smaller than the optimum diameter that had been specified.

## IV.RESULT OF EXPERIMENT

The experiment started with the construction of trees which was done with the use of clock routing algorithms. The analyzed processes for the formation of Thiessen polygons and diagrams were used. A one-level mesh was used. In the construction of the clusters, four clusters were used, and consequently, four trees were built. The four trees were rooted each at its node. 5 circuits were constructed as a benchmark and their composition can be found in http://vlsi-cad.ucsd.edu/GSRC/bookshelf/Slots/BST/. There was the use of 90mn technology chips for this experiment, benchmark specifications for the experiment are the ones used in [19], and a workstation was used. To make the underlying trees for the connection of individual points to clusters, the algorithm discussed in [20] was used. To ensure that there was a minimum delay, there was the assignment of the top-most metal layer to the mesh. For the trees that were tethering the polygons to sinks, they were allocated to lower-level metal layers of metal. Further, there was the use of HSpice in the mesh simulation, which was done to ensure there was a high level of accuracy. The lumped $\pi$-model was used for simulation purposes and it was executed through a product of unit length capacitances and unit lengths for the wires that were used. The testing process was conducted for different values of K.

Figure 4: The skew and delay values for the benchmarks used




One of the findings of the experiment is that that the skewness declined when there was an increase in the number of polygons. Based on the observations made, when there was an increase in the polygons K, there was a consequent increase in the spines on the chip, and this is seen as a contributor to a decline in the skewness and a reduction in delay.

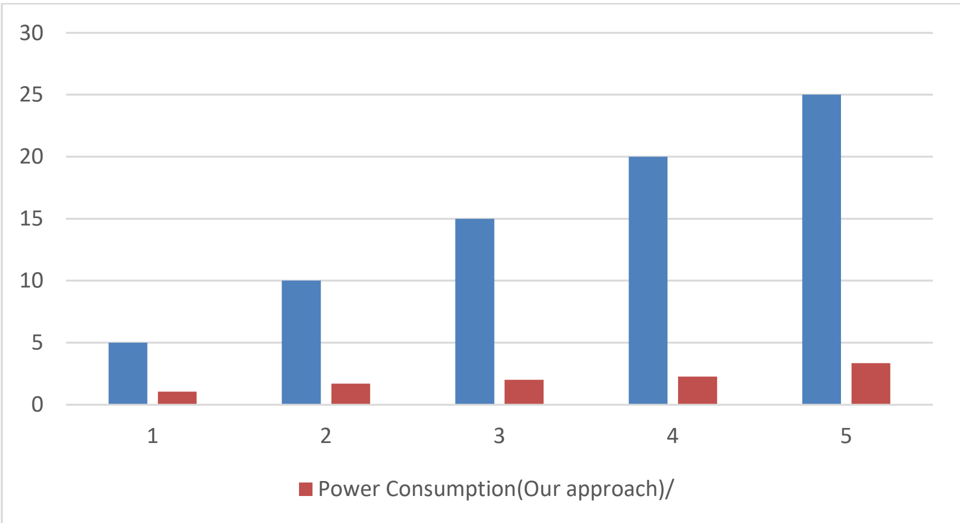
| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.282|

|| Volume 11, Issue 2, February 2022 ||

DOI:10.15662/IJAREEIE.2022.1102001

In a previous study [19], the value of K, which is the cluster size was static and was not variant. However, in this experiment, there was variance in the value of K and as a consequence, there was a variance in delay and skewness as shown in Figure6. In the analysis, it was found that when k was 25 there was a reduction in the skew of 41% for R5. This was replicated in all the other cases, where there was a decline in the skewness whenever there was an increase in K. It was also noted that if there was an increase in the value of K, there was a decline in delay duration as shown in table 1, with consequent delays declining with increasing values of k. However, this design leads to a non-uniform distribution of sinks. This may not be of much consequence since the focus is to have a minimum skewness.
The other analysis done was on the power consumption rate for clusters of different sizes. The results of this analysis are shown in figure7. Based on the analysis, the correlation between power consumption and skewness and delay is that of inverse proportionality. High power consumption led to lower levels of skewness and delay. Conversely, when there is low power consumption, there are higher levels of skewness and delay. The proportion of the increase is dependent on the values of k. When the values that are registered in k are small, then there is a ratio that is larger than 1 and when the value for K is large, there is a large proportionality of the power that is used up. This finding implies that in the design of the network, a designer has the option of making trade-offs between power consumption and skewness. To achieve low skewness, more power is needed and if the designer does not high power consumption, they will have to do with some level of skewness in their design.

Figure 5 : k and power consumptions




## V.CONCLUSION

This research sought to present new advancements to the existing Clock distribution networks. The prototype for the clock distribution network presented is a multi-level mesh-based network. In the design of the upper mesh, there has been the use of Thiessen polygons and Dirichlet tessellation. One of the outstanding aspects of this network is that it takes into account the density of sinks. This prototype has also used HSpice benchmarking circuit. The analysis of the prototype has shown that there it has lower delay and skewness values than that of other porotypes that exist. The design has also been verified to consume far much less power than that consumed by dense mesh. However, apart from the dense mesh, its power consumption may be considerably much higher. The trade-off point for the power consumption that has been established is that of the value of K, which represents the distribution of clock sinks. This is a work in progress and more research is needed on the level of trade-offs that a designer should engage to have optimum power usage while keeping the skewness and the delay at a minimum and possibly at zero level.

## REFERENCES

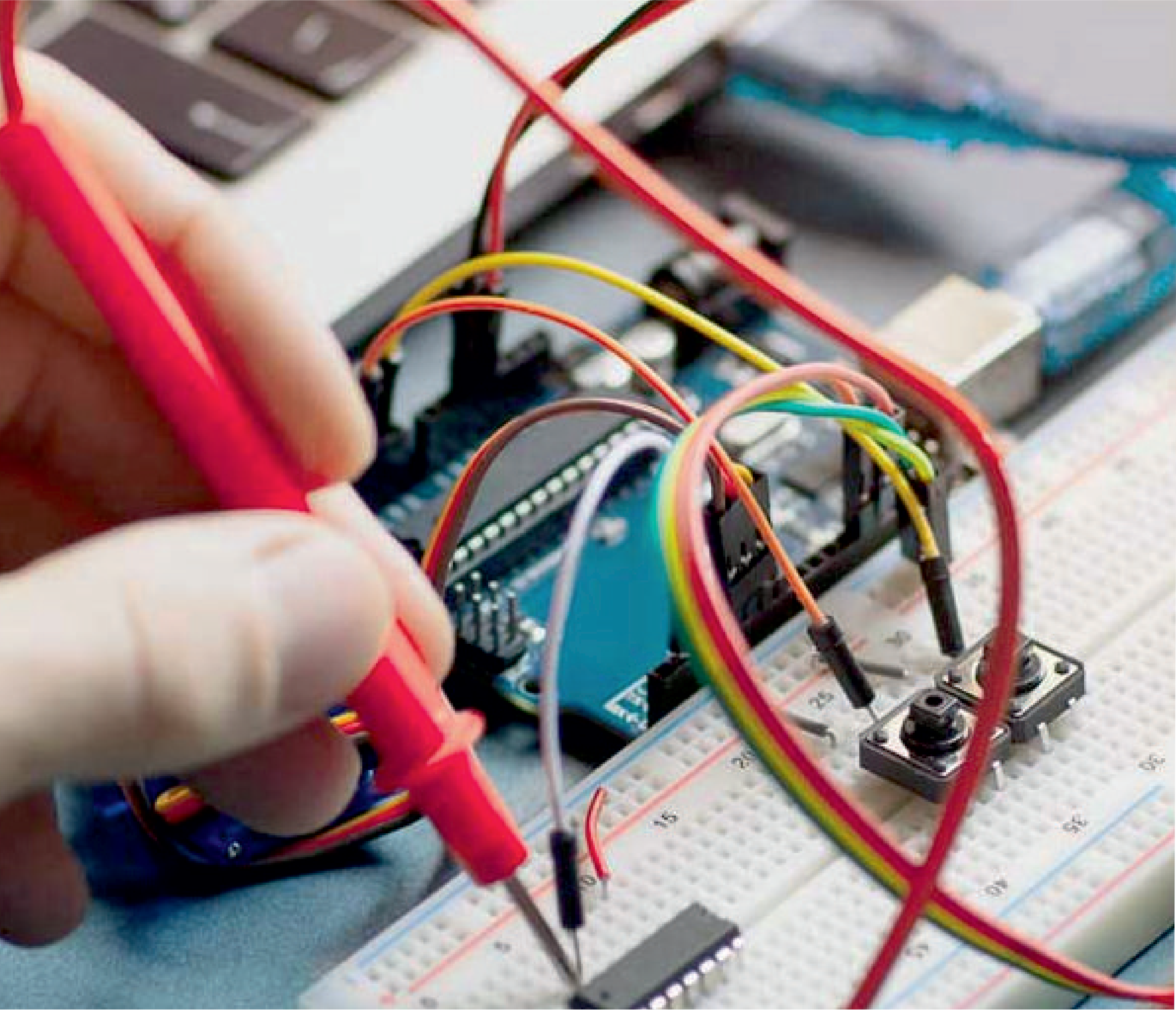
1. V. Agarwal, M. Hrishiksh, S. Keckler, and D. Burger. Clock rate versus IPC. In *Proc. Int. Symp. on Comp. Archi.*, pages 67–74, 2000.
2. F. Aurenhammer. Voronoi diagrams — a survey of a fundamental geometric data structure. In *ACM Comput. Surv.*, volume 23, pages 345–405. ACM Press, New York, 1991.

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.282|

|| Volume 11, Issue 2, February 2022 ||

DOI:10.15662/IJAREEIE.2022.1102001

3. M.de Berg. *Computational Geometry: Algorithms and Applications*. Springer-Verlag, New York, second edition, 2000.
4. A. Caldwell and A. Markov. Toward CAD-IP reuse: The macro GSRC bookshelf of fundamental CAD algorithms. In *IEEE Design and Test*, March 2002.
5. H. Chen and C.K. Cheng. A multi-level transmission line network approach for multi-giga hertz clock distribution. In *Proc. ASP-DAC*, pages 103–106, 2005.
6. T. H. Cormen, C. E. Leiserson, R. L. Rivest, and C. Stein. *Introduction to Algorithms*. MIT Press, Cambridge, MA, second edition, 2004.
7. M. P. Desai, R. Cvijetic, and J. Jensen. Sizing of clock distribution networks for high performance CPU chips. In *Proc. DAC*, pages 389–394, 1996.
8. M. Edahiro. A clustering-based optimization algorithm in zero-skew routings. In *Proc. DAC*, pages 612–616, 1993.
9. H. Edelsbrunner. *Geometry and Topology for Mesh Generation*. Cambridge Univ. Press, New York, first edition, 2000.
10. P. Restle et al. A clock distribution network for microprocessors. In *IEEE Trans. Solid-State Circuits*, volume 36, pages 792–799, May, 2001.
11. E. Friedman. Clock distribution networks in synchronous digital integrated circuits. In *Proc. IEEE*, volume 89, pages 685–692, May 2001.
12. M. F. Hsiao, M. Marek-Sadowska, and S. J. Chen. Crosstalk minimization for multiple clock tree routing. In *Proc. MWSCS*, pages 152–155, 2002.
13. M. A. Jackson, A. Srinivasan, and E. S. Kuh. Clock routing for high performance ICs. In *Proc. DAC*, pages 573–579, 1990.
14. A. Kahng and C. Tsao. Planar-dme: Improved planar zero-skew clock routing with minimum pathlength delay. pages 440–445, 1994.
15. A. B. Kahng and C. A. Tsao. Practical bounded-skew clock routing. In *J. VLSI Signal Process. Syst.*, volume 16, pages 199–215, 1997.
16. N. Kurd, J. Barkatullah, R. Dizon, and T. Fletcher. A multigigahertz clocking scheme for the Pentium 4 microprocessor. In *IEEE Trans. Solid-State Circuts*, volume 36, pages 1647–1653, Nov. 2001.
17. M. Mori, H. Chen, B. Yao, and C.-K. Cheng. A multiple level network approach for clock skew minimization with process variations. In *Proc. ASP-DAC*, pages 263–268, 2004.
18. A. Rajaram, J. Hu, and R. Mahapatra. Reducing clock skew variability via cross links. In *Proc. DAC*, pages 18–23, 2004.
19. H. Su and S. S. Sapatnekar. Hybrid structured clock network construction. In *Proc. ICCAD*, pages 333–336, 2001.
20. R. Tsay. An exact zero skew clock routing algorithm. In *IEEE Trans. CAD*, volume 12, pages 242–249, Feb. 1993.



INNO SPACE
SJIF Scientific Journal Impact Factor
Impact Factor: 7.282

doi crossref

INTERNATIONAL STANDARD SERIAL NUMBER INDIA

निस्केयर
NISCAIR

# International Journal of Advanced Research

## in Electrical, Electronics and Instrumentation Engineering

9940 572 462 6381 907 438 ijareeie@gmail.com

Scan to save the contact details

www.ijareeie.com